ASSIGNMENT 5

Textbook Assignment: "Central Processing Units and Buses," chapter 5—continued, pages 5-13 through 5-23.

5-1. The interrupt that occurs with the actual event that caused the interrupt is (a) what type and (b) what will be the status of the condition of the process or program after the interrupt is processed?

1. (a) Asynchronous
   (b) Different conditions will exist
2. (a) Asynchronous
   (b) The exact same conditions will exist
3. (a) Synchronous
   (b) Different conditions will exist
4. (a) Synchronous
   (b) The exact same conditions will exist

5-2. What type of interrupt occurs (a) when there is an error in a peripheral device and (b) when 1/0 operations are terminated?

1. (a) External (b) internal
2. (a) External (b) external
3. (a) Internal (b) internal
4. (a) Internal (b) external

5-3. In a microcomputer, an interrupt from an internal hard disk can be masked out by the computer.

1. True
2. False

5-4. In microcomputers, which of the following methods can be used to direct the processor to the address of the interrupt of a maskable interrupt?

1. An interrupt code only
2. A ROM lookup table only
3. A ROM/PROM lookup table only
4. An interrupt code and a ROM/PROM lookup table

IN ANSWERING QUESTIONS 5-5 THROUGH 5-11, SELECT FROM THE FOLLOWING LIST THE INTERRUPT CLASS THAT MATCHES THE CONDITION OR PRIORITY DESCRIBED IN EACH QUESTION.

1. Class I
2. Class II
3. Class III
4. Class IV

5-5. An RTC overflow has occurred.

5-6. An intercomputer timeout has occurred.

5-7. The highest priority interrupt that can occur in the computer.

5-8. A power out of tolerance has occurred.

5-9. The computer will execute a power failure processing routine.

5-10. An input chain interrupt has occurred.

5-11. An illegal op code has been executed in the CPU.

5-12. Lower level interrupts can be disarmed and/or armed by software.

1. True
2. False

5-13. All of the following interrupts cannot usually be locked out by software except which one?

1. Power fault
2. External interrupt
3. CPU instruction fault
4. IOC instruction fault interrupt

5-14. In newer computers, which of the following methods can be used to retain multiple interrupt codes of the same class?

1. Interrupt stack only
2. Interrupt queue only
3. Both interrupt stack and queue
4. Index registers

5-15. For an interrupt signal in a particular class to be indicated to the CPU, what minimum number of interrupts must be present?

1. One
2. Two
3. Three
4. Four

A. Terminate current program execution
B. Lock out all interrupts
C. Store program and register data
D. Retrieve interrupt processor data
E. Enter executive state and enable desired interrupts
F. Execute interrupt processor program
G. Return to original process

Figure 5-A.—Interrupt handling process steps,

IN ANSWERING QUESTIONS 5-16 THROUGH 5-23, REFER TO FIGURE 5-A ABOVE AND FIGURE 5-9 ON PAGE 5-13 OF THE TRAMAN. SELECT THE MOST APPROPRIATE INTERRUPT HANDLING PROCESS STEP FOR THE PROCESS DESCRIBED IN EACH QUESTION.

5-16. New interrupts are locked out to protect the integrity of the process that ensures returning to the same conditions after processing the interrupt.

1. A
2. B
3. C
4. D

5-17. The step in which the interrupt process will be initiated.

1. A
2. B
3. C
4. D

5-18. In newer computers, a separate register set for each task and executive state is used, and these registers are disabled and the contents protected until the appropriate state is entered.

1. A
2. B
3. C
4. D

5-19. The computer enters the required executive state and enables the interrupts that in turn interrupt the interrupt processor after the status registers are loaded.

1. B
2. C
3. D
4. E

5-20. The new executive state registers are loaded with the interrupt processor program data after the register data is saved.

1. B
2. C
3. D
4. E

5-21. The current process's register data is stored with at least the contents of the program counter and status register(s).

1. A
2. B
3. C
4. D

5-22. The first instruction of an interrupt routine is executed after sampling interrupt code words.

1. D
2. E
3. F
4. G

5-23. The program counter and status register(s) is/are reloaded with the saved data. The next instruction, prior to the interrupt (instruction 4), is called up by the program counter.

1. D
2. E
3. F
4. G

5-24. It requires less time to access control memory than to access main memory.

1. True
2. False

5-25. Where is cache memory usually located in a computer?

1. In main memory
2. In the I/O section
3. Between the CPU's control and ALU sections
4. Between main memory and the CPU

5-26. For rapid data transfers, what two types of semiconductor devices are usually used by cache memories?

1. Bipolar DRAMs and MOS SRAMs
2. Bipolar SRAMs and bipolar DRAMs
3. MOS SRAMs and MOS DRAMs
4. MOS DRAMs and bipolar SRAMs

5-27. In terms of access and capacity of a cache memory, a cache memory is usually on the order of one magnitude ___(a)___ (slower; faster) than main memory and its capacity is two orders of magnitude ___(b)___ than main memory. (less; more)

1. (a) Slower (b) less
2. (a) Slower (b) more
3. (a) Faster (b) less
4. (a) Faster (b) more

5-28. Which of the following methods can be used by a cache memory to indicate which entries of main memory have been copied into it?

1. A hit
2. A tag store
3. An identifier
4. Both 2 and 3 above

5-29. Which of the following is/are properties of cache memory?

1. A high-speed memory
2. A logical network and an old entries replacement method
3. Timing and control
4. Each of the above

5-30. To indicate that data from the requested address is present, which, if any, of the following terms is used?

1. Hit
2. Miss
3. Tag
4. None of the above

5-31. What area of cache memory writes only to the directories?

1. Updates
2. Invalidates
3. Searches
4. Tags

5-32. What cache process is performed by a requestor other than the CPU within?

1. Main
2. Mapping
3. Eavesdrop
4. Searching

IN ANSWERING QUESTIONS 5-33 THROUGH 5-36, SELECT FROM THE FOLLOWING LIST THE CACHE MAPPING TECHNIQUE DESCRIBED IN EACH QUESTION.

1. Direct mapping
2. Fully associative mapping
3. Set associative mapping

5-33. Is the most flexible cache mapping technique with regards to where data can reside.

5-34. Combines the best cache mapping techniques.

5-35. Main memory locations can only be copied into one location in cache.

5-36. If cache is fill, a replacement algorithm is used to decide which block gets replaced by new data.

5-37. What cache read method can be used to present the cache and main memory with the reference simultaneously?

1. Look-aside, serial read
2. Look-aside, parallel read
3. Look-through, serial read
4. Look-through, parallel read

5-38. In a look-through read, the cache is checked last.

1. True
2. False

5-39. Optimum cache replacement would be psychic and have perfect knowledge of the future. What cache replacement policy, if any, comes closest to the optimum cache replacement?

1. LRU
2. FIFO
3. Random
4. None, all are very different

5-40. Instruction routines in a ROM are considered to have which of the following characteristics?

1. Permanent and volatile
2. Permanent and nonvolatile
3. Temporary and volatile
4. Temporary and nonvolatile

5-41. Permanent software loaded as firmware is the process known by which of the following terms?

1. Boot
2. Bootstrap
3. Boot Up
4. Each of the above

5-42. An NDRO in a militarized mainframe or minicomputer is usually located in which of the following places?

1. In the CPU module
2. In the chassis that contains CPU's pcbs
3. Either 1 or 2 above, depending on whether it is a mini or mainframe computer
4. On one or more IC chips of a CPU/memory pcb

5-43. Diagnostics programs on an NDRO include all of the following items except which one?

1. Test the timer
2. Load failure analysis
3. Memory and interface tests
4. Computer interconnection system

IN ANSWERING QUESTIONS 5-44 THROUGH 5-47, SELECT FROM THE FOLLOWING LIST THE AREA OF A BIOS DESCRIBED IN EACH QUESTION.

1. Diagnostic testing
2. Environmental inventory
3. Boot procedure

5-44. Testing the video, interrupt controller, CPU register and flags, or the keyboard.

5-45. A prompt is displayed to let you know the microcomputer is ready to use.

5-46. The ROM chip program searches for the operating system files.

5-47. The number of printers and serial ports are determined.

5-48. The ALU obtains the data required to perform arithmetic and logical calculations from which of the following places?

1. Timing circuits
2. Operands only
3. Designated CPU registers only
4. Operands and designated CPU registers

5-49. To perform computations, which of the following methods are used in addition and subtraction operations?

1. Radix minus one only
2. Radix minus two only
3. Conversion only
4. Radix minus one, radix minus two, and conversion

5-50. The destination of the results of ALU operations may include which of the following places?

1. Timing circuits
2. Registers only
3. Operands only
4. Registers and operands

5-51. Computers can be designed to use which of the following word-length operands to carry out arithmetic operations?

1. Whole-word, half-word, and quarter-word operands only
2. Single-length word operands only
3. Double-length word operands only
4. Whole-word, half-word, quarter-word, single-length word, and double-length word operands

5-52. Double-length memory word operands will be used for mathematical operations when the size of the result would be (a) _____ (less; greater) than the length of either of the registers used to provide inputs to the ALU or the operands being input to the ALU are _____ (b) _____ than a single word. (larger; smaller)

1. (a) Less (b) larger
2. (a) Less (b) smaller
3. (a) Greater (b) larger
4. (a) Greater (b) smaller

IN ANSWERING QUESTIONS 5-53 THROUGH 5-56, SELECT FROM THE FOLLOWING LIST THE ITEM USED BY THE ALU IN ARITHMETIC OR LOGICAL CALCULATIONS DESCRIBED IN EACH QUESTION.

1. Flags
2. Selectors
3. Counters

5-53. Used to keep track of shifts.

5-54. A carry or borrow condition is indicated.

5-55. Used to transfer data between various registers in the ALU.

5-56. Used to indicate the status of the last logical calculation.

5-57. What method is used to represent a integer number?

1. R's minus 1
2. R's minus 2
3. Fixed-point
4. Floating-point

5-58. For whole numbers, what is the maximum absolute decimal value that can be contained in a 6-bit register?

1. 31
2. 32
3. 63
4. 64

5-59. A zero in what (a) position indicates a positive number and a one in what (b) position indicates a negative number?

1. (a) msb (b) 1sb
2. (a) msb (b) msb
3. (a) lsb (b) lsb
4. (a) lsb (b) msb

5-60. In a 6-bit register, the largest positive value that can be contained is what decimal number?

1. 31
2. 32
3. 63
4. 64

5-61. When floating-point operations are performed, the radix point must be aligned properly. The alignment of the radix point takes place at which of the following times?

1. During arithmetic operations only
2. After arithmetic operations only
3. Either during or after arithmetic operations, depending on the type of operation
4. Before arithmetic operations

5-62. In floating-point operations, what is the fractional portion of the number called?

1. Characteristic
2. Mantissa
3. Radix
4. Sign

5-63. In a number, the radix point is usually placed in what location?

1. Between the sign bit and the msb of the characteristic
2. Between the sign bit and the lsb of the characteristic
3. Between the sign bit and the lsb of the mantissa
4. Between the sign bit and the msb of the mantissa

IN ANSWERING QUESTION 5-64, REFER TO FIGURE 5-15, FRAME A, ON PAGE 5-21 IN THE TRAMAN.

5-64. For which of the following reasons is zero extended through the most significant 16 bits of the word that contains the characteristic?

1. The integer is a positive number
2. The integer is a negative number
3. The mantissa is a positive number
4. The mantissa is a negative number

5-65. Where the most accuracy is required during floating-point operations, (a) what format is used with two 32-bit words and (b) what is the relationship of the characteristic to the mantissa?

1. (a) Single-precision
   (b) Characteristic is smaller
2. (a) Single-precision
   (b) Characteristic is larger
3. (a) Double-precision
   (b) Characteristic is smaller
4. (a) Double-precision
   (b) Characteristic is larger

5-66. Under which of the following conditions are the mantissa's results rounded up?

1. When the mantissa is less than one-half of one only
2. When the mantissa is greater than one-half of one only
3. When the mantissa is equal to or less than one-half of one
4. When the mantissa is equal to or greater than one-half of one

5-67. What type of floating-point interrupt condition, if any, exists when there is a positive excess?

1. Overflow
2. Underflow
3. Divisor
4. None, there is no floating point interrupt

5-68. What method does the ALU use to perform arithmetic and logical instructions?

1. Logical quotients of the logic gates
2. Logical products of the logic gates
3. Logical sums of the logic gates
4. Logical differences of the logic gates

5-69. The ALU portion of a computer can be designed to perform a wide variety of arithmetic operations. Which of the following are the only arithmetic capabilities that computers can have to perform all arithmetic operations?

1. Addition and multiplication
2. Addition and subtraction
3. Subtraction and multiplication
4. Subtraction and division

5-70. A computer has no dedicated square root instruction. Which of the following instructions could be used to perform the square root function?

1. Addition and subtraction only
2. Addition and comparison only
3. Subtraction and comparison only
4. Addition, subtraction, and comparison

5-71. Logical ALU functions include all of the following except which one?

1. AND and OR
2. NOT
3. Compare
4. BAM

5-72. A numeric data coprocessor operates in (a) what manner with the CPU and independent of the CPU using (b) which of the following buses?

1. (a) Parallel
   (b) Different buses from the CPU
2. (a) Parallel
   (b) The same buses as the CPU
3. (a) Serial
   (b) Different buses from the CPU
4. (a) Serial
   (b) The same buses as the CPU